Docket No.: X2850.0015

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yoshiaki Shiota

Application No.: 09/220,434 | Confirmation No.: 3503

Filed: December 24, 1998 | Art Unit: 2665

For: FRAME - RELAY FRAME TRANSMISSION CIRCUIT | Examiner: T. D. Tran

APPEAL BRIEF

U.S. Patent and Trademark Office
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Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on January 18, 2005, and is in furtherance of said Notice of Appeal.

You are hereby authorized to charge our credit card for the fee of $500.00 required under Section 1.17(f). PTO Form 2038 is attached.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2215.

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CONTINGENT EXTENSION REQUEST

If this communication is filed after the shortened statutory time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 CFR 1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 CFR 1.135. The fee under 37 CFR 1.17 should be charged to our Deposit Account No. 50-2215.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

NEC Corp.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 11 claims pending in application.

B. Current Status of Claims

1. Claims canceled: none
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1-11
4. Claims allowed: none
5. Claims rejected: 1-11

C. Claims On Appeal

The claims on appeal are claims 1-11

IV. STATUS OF AMENDMENTS

Applicant filed a Response After Final Rejection on October 29, 2004. The Examiner responded to the Response After Final Rejection in an Advisory Action mailed December 28, 2004. In the Advisory Action, the Examiner

indicated that Applicant's request for reconsideration did not place the application in condition for allowance.

Accordingly, the claims enclosed herein as Appendix A incorporate all of the amendments to the claims made during the pendency of this case.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a frame-relay frame transmission circuit that reduces overhead caused by converting, for example, a frame-relay frame into an asynchronous transfer mode (ATM) cell. See, Specification at 3.

When a frame-relay frame header is converted into an ATM Adaptation Layer 5 (AAL5) header, the AAL5 header is larger than the header for other protocols. See, Specification at 2. In the prior art, to perform this conversion, the frame data and its related header data were written into a frame buffer. See, Specification at 2, lns. 3-11. Once the header and data were first written into memory the header was decoded. If the converted header was larger than the original header, the frame data was written into a free memory area so that the converted header would not overwrite the frame data. See, Specification at 2, lns. 12-20.

In order to reduce overhead, a frame-relay frame transmission circuit of the present invention writes a received frame-relay frame into a memory location shifted from the top of a frame buffer. It should be noted that there are multiple frame buffers in memory 16, as shown in Fig. 5. The particular shift from the top of a frame buffer is determined for each connection. See, Specification at 3, lns. 12-16. According to the specification, the frame receiver 10 (shown in Figure 3) searches for an available frame buffer (shown in Figure 5). See, Specification at

6. The frame, however, is not written to the first available address 21 in the frame buffer as was done in the prior art. See, Figure 5. Instead, the frame is written to an address shifted from the first available address 22 in the frame buffer. Id. The purpose of the shifted memory location is to accommodate the converted AAL5 header. See, Specification at 4, lns. 15-22. Figure 5, which depicts a frame that is written from a position shifted from the first available address in a frame buffer, clearly shows that the frame is written to a memory location 22 that is shifted from a top 21 of the next available memory location in the frame buffer.

The disclosed frame relay circuit for reassembling a frame-relay frame into an ATM cell comprises a processor, a frame receiver, a memory, and a segmentation and reassembling device. See, Specification at 3, Fig. 3. A frame receiver 10 receives the frame. The processor 14, shown in Fig. 5, determines the amount the frame is to be shifted from a top of the next available memory location 21 in a frame buffer to accommodate the larger converted header. See, Specification at 5, Figs. 3. The required shift is dependent upon the specific connection. Specification at 3, ln. 16. The frame is then stored in one of the frame buffers in the memory 16 at a location 21 shifted from the top of the next available memory location in the frame buffer by said shift size. Figs. 4, 5. The converted header is then written into the memory location at the top of the frame buffer, including the shifted memory amount. Finally, the segmentation and reassembling device 17 reassembles the frame into the ATM cell.

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

Applicant requests review of the final rejection of claims 1-3, 6, and 9 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the rejection asserts that the limitation "writes said frame to a memory location shifted from a top of the next available memory location" is not disclosed in the specification.

Applicant requests review of the final rejection of claim 1 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 6,144,699 ("Williams").

Applicant requests review of the final rejection of claims 2-11 under 35 U.S.C. § 103(a) as being unpatentable over Williams in view of U.S. Patent No. 6,301,259 ("Nakabayashi").

VII. ARGUMENT

Claims 1-11 are pending and have been examined in the present application. All of the claims are in condition for allowance and any pending rejections should be withdrawn. Applicant is mainly addressing independent claims 1, 3, 6, and 9 in this brief.

A. Claims 1-3, 6, and 9 each meet the requirements of 35 U.S.C. § 112, first paragraph

Paragraph 2 of the July 15, 2004 Office Action finally rejected claims 1-3, 6, and 9 under 35 U.S.C. § 112, first paragraph. The Examiner objected to the phrase "writes said frame to a memory location shifted from a top of the next available memory location in a frame buffer." The Examiner asserted that this limitation is not described in the specification in such a way as to enable one

skilled in the art to make and/or use the invention. Applicant asserts that this rejection is improper.

Under 35 U.S.C. § 112, first paragraph, the specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains or with which it is most nearly connected, to make and use the same. This language contains both the written description and enablement tests for sufficiency of the specification's disclosure.

For compliance with the written description requirement of 35 U.S.C. § 112 there must be sufficient information in the original disclosure to show that the inventor possessed the invention at the time of the original filing. See, Moba B.V. v. Diamond Automation Inc., 325 F.3d 1306, 1320 (citing Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 1561 (Fed. Cir. 1991)). The written description possession test is performed "from the viewpoint of one of skill in the art." See, Moba, 325 F.3d at 1321.

In the present case, there is sufficient disclosure in the specification and figures to establish that the inventor possessed the invention at the time of the original filing, and further, one skilled in the art can reproduce Applicant's claimed invention. Support for the above quoted limitation in the independent claims may be found on page 3, line 11 through page 6, line 10 and Figures 4 and 5. The referenced portions of the specification disclose writing the frame to a memory location shifted from a top of the next available memory location in a frame buffer.

The specification states that "in order to accomplish the above object, in a frame-relay frame transmission circuit of the present invention, when a received frame-relay frame is written in a memory, the frame is written from an address shifted from the top of a frame buffer. The shift size is determined for each connection." See, Specification at 3. As shown in Figure 5, the frame is shown shifted from the top of a frame buffer i.e., shifted from the top of the next available memory location. The reason the shift is required, as discussed infra in Section V, is that the converted AAL5 header will overwrite the frame data if the data is not moved.

Frame receiver 10 (shown in Figure 3) searches for a frame buffer (shown in Figure 5). See, Specification at 6. The frame data, however, is not written to the first available address 21 in the selected frame buffer. See, Figure 5. Instead, the frame data is written to an address shifted from the first available address 22 in the frame buffer, e.g., the top of the frame buffer. Id. Thus, Figure 5, which depicts a plurality of frame buffers, shows a frame which is written from a position shifted from the first available address in a frame buffer. Thus, the frame is written to a memory location 22 that is shifted from the top of the frame buffer.

Because the specification and drawings clearly disclose the limitation "writes said frame to a memory location shifted from a top of the next available memory location", Applicant assert that the rejection under 35 U.S.C. § 112, first paragraph, is improper and must be withdrawn.

It should be noted that claims 4, 5, 7-8, and 10-11 depend from the claims that were rejected under 35 U.S.C. § 112, first paragraph, however, they

were not rejected. Applicant's assert that either all of the claims or none of the claims must suffer from the Examiner's rejection. Since some of the dependent claims are not rejected, none of the claims should be rejected. If the rejection is redrafted to include all of the claims, the rejection is improper for the reasons discussed above.

B. Claim 1 is not anticipated by Williams

Paragraph 3 of the Office Action rejects claim 1 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 6,144,669 ("Williams"). Because Williams fails to disclose each and every limitation in claim 1, claim 1 must be allowed.

To anticipate a claim under 35 U.S.C. § 102, the cited reference must disclose every element of the claim, as arranged in the claim, and in sufficient detail to enable one skilled in the art to make and use the anticipated subject matter. See, PPG Industries, Inc. v. Guardian Industries Corp., 75 F.3d 1558, 1566 (Fed. Cir. 1996); C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1349 (Fed. Cir. 1998). A reference that does not expressly disclose all of the elements of a claimed invention cannot anticipate unless all of the undisclosed elements are inherently present in the reference. See, Continental Can Co. USA v. Monsanto Co., 942 F.2d 1264, 1268 (Fed. Cir. 1991).

Among the limitations of independent claim 1 not present in the cited reference is wherein said device receives a frame-relay frame and writes said frame to a memory location shifted from a top of the next available memory location in a frame buffer.

Williams discloses a system which includes a first-in/first-out (FIFO) queue. (Col. 9, lns. 42-45.) The processor 84 in Williams retrieves frames from the queues for processing in a concurrent round-robin fashion, the frames having been placed at the tail of the queue. (Col. 12, lns. 40-49.) At best, the Williams system stores the frame data in the next available memory location in the queue. But, there is no disclosure whatsoever in Williams that its system shifts the writing of the frame data from the next available memory location. Thus, there is no disclosure of the frame being written to a memory location shifted from a top of the next available memory location in the frame as explicitly recited in claim 1. Therefore, Williams fails to anticipate claim 1. As such, Applicant respectfully requests reconsideration and allowance of claim 1[1].

C. Claims 2-11 are patentable over Williams in view of Nakabayashi

Claims 2-11 were improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams in view of U.S. Patent No. 6,301,259 ("Nakabayashi"). Applicant respectfully requests reconsideration and withdrawal of this rejection.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or combine references to arrive at the claimed subject matter. The prior art references must also teach or suggest all the limitations of the claim in question. See, M.P.E.P. § 706.02(j). A reference can only be used for what it clearly discloses or suggests. See, In re Hummer, 113 U.S.P.Q. 66 (C.C.P.A. 1957); In

[1] Claim 2 depends from, and contain all the limitations of claim 1. This dependent claim also recites additional limitations which, in combination with the limitations of claim 1, are neither disclosed nor

re Stencel, 4 U.S.P.Q.2d 1071, 1073 (Fed. Cir. 1987). Here, the references, whether taken individually or in combination, do not disclose or suggest the invention claimed by the Applicant.

Each of Applicant's independent claims 1, 3, 6, and 7 include the limitation that the frame is written to a memory location shifted from the top of the next available memory location in a frame buffer. As discussed above, with respect to claim 1, the Williams reference fails to disclose this limitation. Nakabayashi was included to show additional limitations recited in claims 2-11, but Nakabayashi fails to cure the basic deficiency in Williams discussed above. Even if combined, the teachings of Nakabayashi and Williams do not read on the present as recited in claims 2-11. As such, Applicant asserts that claims 2-11 are patentable over the cited combination and request reconsideration and allowance of the pending claims.

Applicant has responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Applicant on December 17, 2004, no further amendments were made to the claims.

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suggested by Williams and is also believed to be directed towards the patentable subject matter.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: April 29, 2005

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/220,434

Claim 1. A frame-relay frame processing device for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell, wherein said device receives a frame-relay frame and writes said frame to a memory location shifted from a top of the next available memory location in a frame buffer.

Claim 2. A frame-relay frame processing device according to claim 1, wherein a size of the shift from the top of the next available memory location in the frame buffer is determined for each connection.

Claim 3. A frame relay circuit for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising:

a processor for determining for each connection a size of a shift by which said frame is to be shifted from a top of the next available memory location in a frame buffer;

a frame receiver for receiving said frame through said connection;

a memory for storing said received frame at a location shifted from the top of the next available memory location in the frame buffer by said shift size; and a segmentation and reassembling device for reassembling said frame into said ATM cell.

Claim 4. A frame relay circuit according to claim 3, wherein, for each connection, said processor writes a data link connection identifier (DLCI) and

said shift size into a connection table, and retrieves said shift size from said connection table using said DLCI as a key.

Claim 5. A frame relay circuit according to claim 3, wherein said frame received by said frame receiver is transmitted to said memory through direct memory access.

Claim 6. A method for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising the steps of:

determining a shift size for each connection by which said frame is to be shifted from a top of the next available memory location in a frame buffer;

receiving said frame and writing said frame starting from an address shifted by said shift size; and

reassembling said frame into an ATM cell.

Claim 7. A method according to claim 6, further comprising the steps of:

writing a data link connection identifier (DLCI) and said shift size into a connection table for each connection; and

retrieving said shift size from said connection table using said DLCI as a key.

Claim 8. A method according to claim 6, wherein said received frame is transmitted to said memory through direct memory access.

Claim 9. A computer readable medium containing program instructions for reassembling a frame-relay frame into an Asynchronous Transfer Mode

(ATM) cell, the program instructions including instructions for performing the steps comprising:

determining a shift size for each connection by which said frame is to be shifted from a top address of the next available memory location in a frame buffer;

receiving said frame and writing said frame starting from an address shifted by said shift size; and

reassembling said frame into an ATM cell.

Claim 10. A computer readable medium according to claim 9, wherein said program instructions include instructions for:

writing a set of a data link connection identifier (DLCI) and said shift size into a connection table for each connection; and

retrieving said shift size in said connection table using said DLCI as a key.

Claim 11. A computer readable medium according to claim 9, wherein said received frame is transmitted to said memory through direct memory access.